APPLICATION NOTE

- TDA8761AM -
9-BIT A/D CONVERTER
DEMONSTRATION BOARD

AN/98096

UPDATE

Philips
Semiconductors

PHILIPS

APPLICATION NOTE

- TDA8761AM -
9-BIT A/D CONVERTER
DEMONSTRATION BOARD

AN/98096

Author:
Stéphane JOUIN

Application Laboratory - PARis
FRANCE

Keywords:
TDA8761AM
Demoboard
9-bit ADC
Digital video

Date: October 1998

REVISION HISTORY

REVISION	DATE	EDITOR	REFERENCE	REMARKS
1.0	July 1998	Stéphane JOUIN	AN/98075	First version with same title

Users are responsible for ensuring that they use the correct version of this document.

CONTENTS

SUMMARY

The **TDA8761** is a 9-bit **A**nalog-to-**D**igital **C**onverter designed for professional video and for other applications. It converts the analog input signal into 9 bits binary digital words or into two's complement digital words at a maximum sampling rate of 40Msps. The reference voltage of the quantization ladder is external.

Only one version of this device exist: it is the **TDA8761AM**, corresponding to the clock frequency of 40Msps.

This **A**pplication **N**ote describes the design and the realization of the **Demonstration Board** (n° 625) using the **TDA8761AM** version with an application environment.

1. MAIN FEATURES OF THE TDA8761AM:

The **TDA8761AM** is a 9-bit **A**nalog-to-**D**igital **C**onverter. It can convert a typical analog input signal into 9 bits binary coded digital words at a maximum sampling rate of 40 Mega sample per second with a typical power dissipation of 158mW. The **TDA8761AM** codes either binary or two's complement digital words with 3V to 5.25V digital outputs. On **Figure 1** are shown the block diagram and the main specification points of **TDA8761AM** device.

- Clock frequency: 40Msps
- Output voltage: 0V - 3V to 5.25V.
- Power dissipation (typical): 158mW.
- Accuracy: 9-bit.
- Supply: 5V with output stages going from 3V to 5.25V.
- Compatibility: inputs: TTL and CMOS,
  outputs: TTL, CMOS (3V to 5.25V).
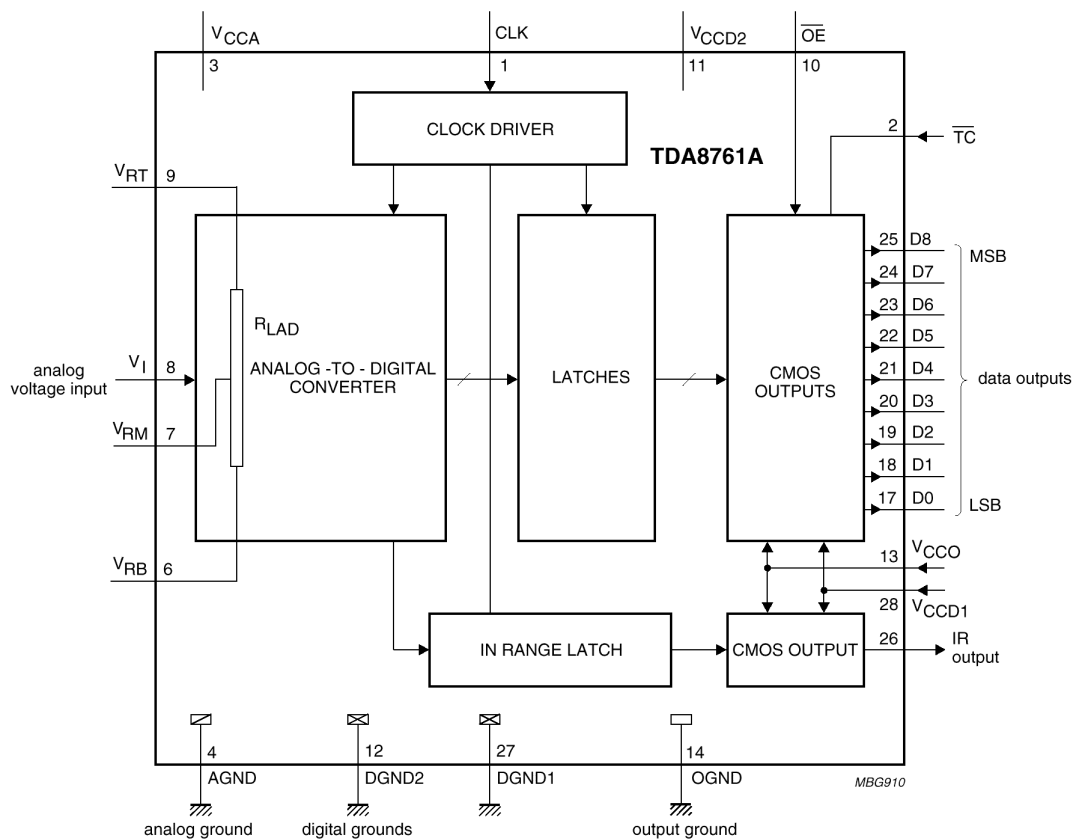
- Figure 1. TDA8761AM block diagram -

2. PRINCIPLE AND DESCRIPTION OF THE BOARD:

On **Figure 2** is shown the principle of the **Demo**nstration **Board** which is described in this **A**pplication **N**ote.
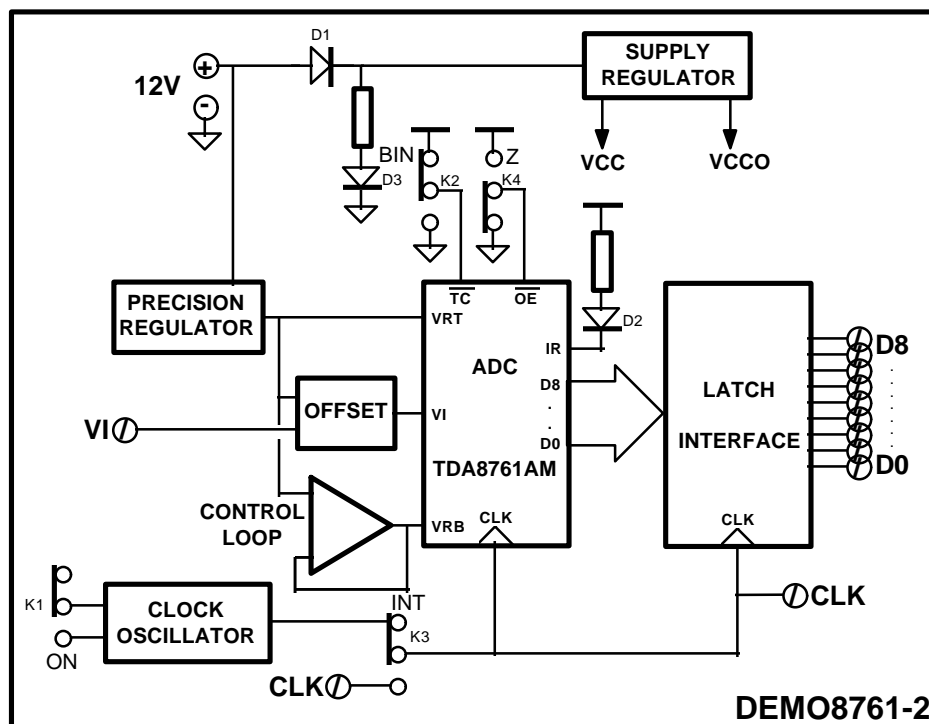
- Figure 2. Functional block diagram of the Demoboard -

The different blocks of the **Demoboard** are:

- A power **supply regulator** used to supply all the circuitry on the board.

- A voltage **precision regulator** supplying the ADC reference voltage TOP input V_{RT} and polarizing the control loop and the input bridge offset.

- A voltage **control loop** circuit making the ADC reference voltage BOTTOM input V_{RB} of the quantization ladder, allowing to compensate the different thermal variations of the voltage values.

- A control **<u>offset</u>** bridge polarizing the ADC analog voltage input VI.

- A **<u>latch interface</u>** synchronizing the ADC data output.

- A **<u>clock oscillator</u>** producing an internal clock on the **Demoboard**.

The **Demoboard** works with a single $+12V_{DC}$ external power supply. All circuitry is protected from reverse polarity. The good supply plugging is indicated by the green LED.

The overflow and the underflow of the input analog signal **VI** is indicated by the red LED.

The sample clock signal on the **Demoboard** can be internal or external by plugging the square generator in the **CLK** SMA connector. In this case, the output impedance of this generator must be 50Ω.

To avoid the crosstalk when an external CLK is used, do not forget to switch off the clock oscillator.

3. OVERVIEW OF THE BOARD:

On **Figure 3** is shown the whole implantation of this **Demoboard**.
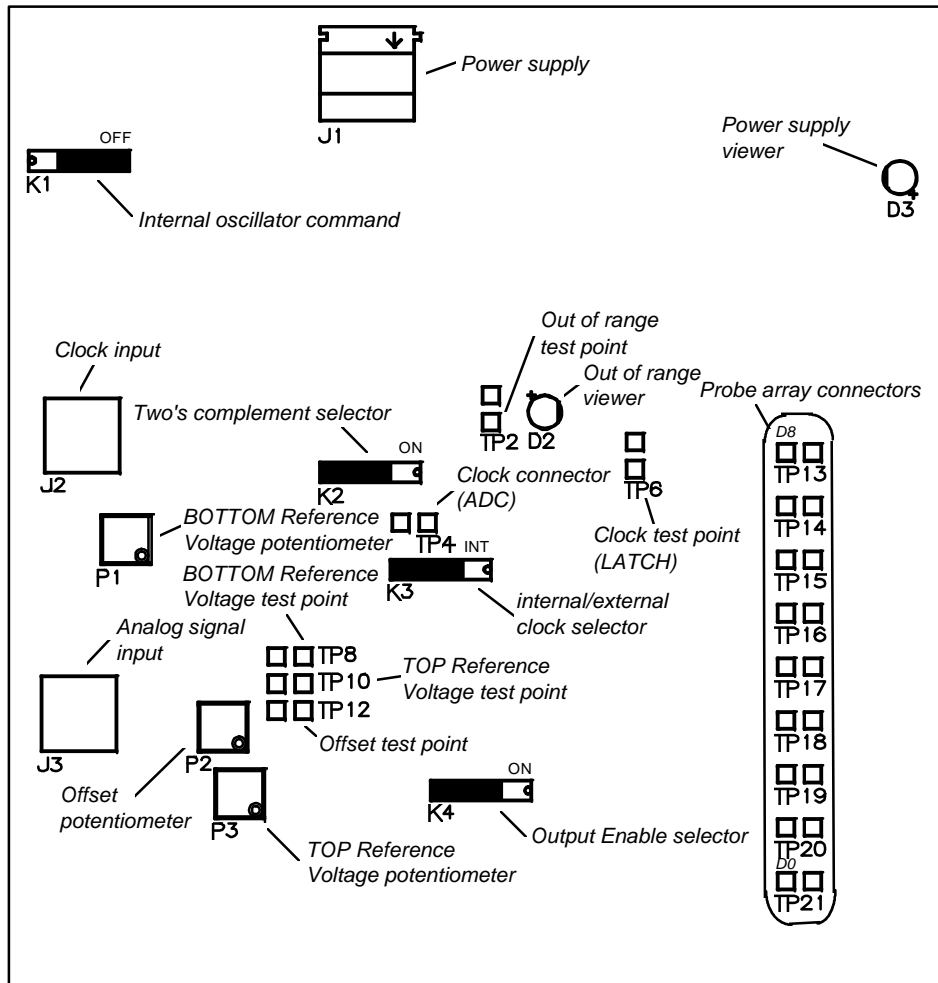
DEMO8761A_2-625

- Figure 3. Overview of Demoboard -

The different connectors, potentiometers, switches, lights and test-points available on the board are:

- **For the general power supply:**

1. A two-points PHOENIX connector **J1** for **12V$_{DC}$** and **GND**.
2. A green light **D3** to indicate the good supply plugging.

- **For the DC voltage adjustment values:**

1. Three chip potentiometers **P3**, **P1** and **P2** to adjust respectively the **V$_{RT}$** TOP reference voltage, the **V$_{RB}$** BOTTOM reference voltage and the **VI$_{DC}$** analog input offset of the ADC.
2. Three test-points **TP10**, **TP8** and **TP12** to control respectively the **V$_{RT}$** and **V$_{RB}$** reference voltages and **VI$_{DC}$** values.

- **For the evaluation of the TDA8761AM:**

1. A SMA **J3** connector with 50Ω for the analog input signal **VI**.
2. A SMA **J2** connector with 50Ω for the external clock input **CLK**.
3. A switch **K4** to enable the ADC outputs by the input $\overline{OE}$.
4. A switch **K2** to choose the ADC two's complement input $\overline{TC}$.
5. A red light **D2** associated with the **TP2** to indicate the out of range of the input analog signal.

- **For the reconstruction of the analog input waveform:**

1. Nine-probe array connectors **TP13** to **TP21** corresponding to the ADC digital output **D8** to **D0** are available to connect the logic analyser which computes the data.
2. A connector **TP4** corresponding to the ADC clock.
3. A test-point **TP6** corresponding to the latch interface clock.

4. PCB DESIGN:

The design is made on a multilayer **P**rinted **C**ircuit **B**oard. On **Figure 4** is given the technological concept used to make this PCB.
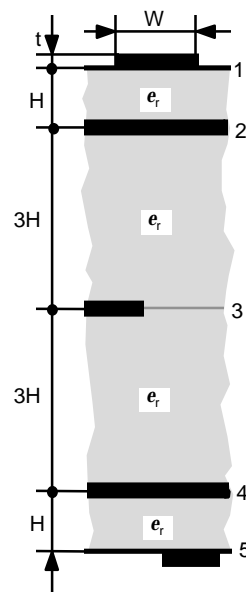
- Figure 4. PCB structure -

Five physical copper layers are used. The first and fifth layers are the signal layers which contain the microstrip lines. The second and fourth layers constitute the ground planes corresponding to the signal layers. The third layer is designed specially for the power supply wires.

The metallic hole technique is employed to make all the necessary interconnections between the layers. The dielectric substrate used is an Epoxy Glass resin with a relative permittivity (e_r) of 4.7 and a copper thickness (**t**) of 35μm (≈1.4mils). The substrate thickness (**H**) is ≈0.2mm (8mils) between the copper layers.

4.1 MICROSTRIP LINES:

To calculate the width (**W**) of these 50Ω matched lines, the Kaup's relation is used:

$$W = \frac{5.98H}{0.8e^{\frac{Zo\sqrt{e_r+1.41}}{87}}} - \frac{t}{0.8} \ ,$$

(Accurate to within 5% when $0.1 < \dfrac{W}{H} < 3.0$ and $1 < e_r < 15$).

where:

$Zo = 50\Omega$, $t = 35\mu m/\approx 1.4mils$, $H = 8mils/\approx 0.2mm$, $e_r = 4.7$.

4.2 POWER SUPPLY WIRE:

To reduce the voltage fluctuation effects due to switching currents inside the integrated circuits, the power supply wires are designed with a low characteristic impedance of microstrip lines in order to obtain a small equivalent inductance.

4.3 ANALOG AND DIGITAL RETURN GROUND POINT:

To minimize the noise due to capacitive coupling between the analog input and the digital output parts of the ADC, two separate ground planes are designed on all layers and are connected together under the device.

5. SPECIAL FEATURES OF THE APPLICATION BOARD:

On **Figure 5** is given the recommended application diagram to obtain optimal performances.
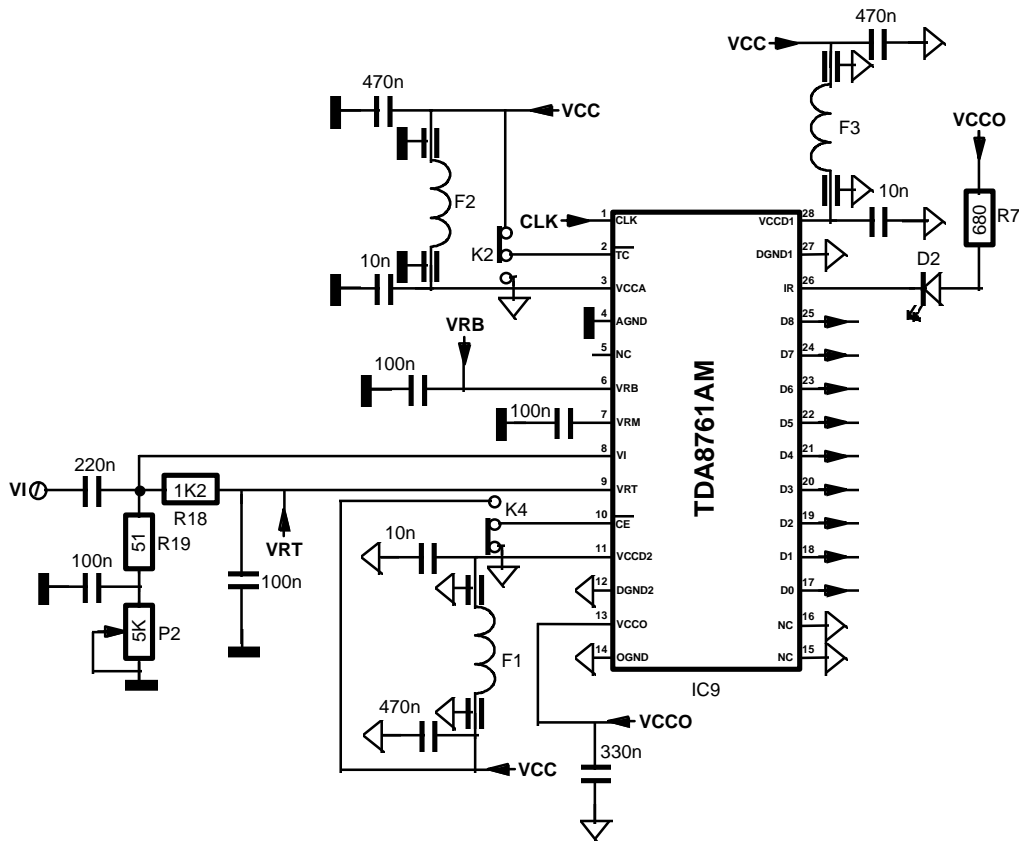
- Figure 5. TDA8761AM application diagram -

5.1 ADC ANALOG INPUT VI:

The DC offset voltage is fixed on the board by an intermediate resistor bridge made by the resistors **R12** and **R13** associated with the potentiometer **P1**. The DC offset voltage value is adjusted on the board from the V_{RT} reference voltage. This reference voltage is supplied by the precision regulator.

So, the V_{OFS} typical offset voltage value (which corresponds to code 255/256) is obtained approximately from the relation:

$$V_{OFS} = \frac{V_{RT} + V_{RB} - V_{OST} + V_{OSB}}{2},$$

where:

$$V_{RT} = 3.43V,$$
$$V_{RB} = 1.3V,$$
$$V_{OST} = V_{OSB} = 0.16V.$$

Hence, the typical DC offset level V_{OFS} corresponding to code 255/256 is:

$$\mathbf{V_{OFS} = 2.365V}.$$

To ensure a sufficient analog input stability, the offset resistor bridge current I_{VI} was fixed at 1mA. The value of **P2** is obtained by:

$$R19 + P2 = R18.\left(\frac{V_{OFS}}{V_{RT} - V_{OFS}} \right) \text{ and } R18 = \frac{V_{RT} - V_{OFS}}{I_{VI}},$$

where:

$$R19 = 50\Omega.$$

The dynamic analog input is connected through a 220nF AC coupling to the external generator through a 50Ω microstrip line and a **R19** = 50Ω resistor ending.

A high frequency decoupling of 100nF was added to the potentiometer **P2** to get a good dynamic ground.

The peak-to-peak magnitude nominal value $VI_{p.-p}$ of the dynamic input signal was determined from the relation:

$$VI_{p.-p} = V_{RT} - V_{RB} - V_{OST} - V_{OSB},$$

hence,

$$\mathbf{VI_{p.-p} = 1.81V}.$$

The quantum of the **TDA8761AM** is:

$$\mathbf{q = \frac{VI_{p.-p}}{2^9 - 1}},$$

hence,

$$\mathbf{q \approx 3.54mV}.$$

5.2 DATA OUTPUT D0 TO D8:

All data outputs of the **TDA8761AM** are CMOS compatible and they are directly addressed to a latch interface circuit.

The switch **K2** corresponding to the two's complement input $\overline{TC}$ allows the choice between the binary digital words or the two's complement digital words.

The switch **K4** corresponding to the output enable input $\overline{OE}$ allows either to enable or to put high impedance on the data outputs.

5.3 DATA RANGE OUTPUT IR:

The underflow and overflow **IR** output pin is directly connected to the red light LED **D2**. When the underflow or overflow of the **VI** analog input signal is detected, the red LED is switched on. On **Figure 6** is shown the functional diagram.
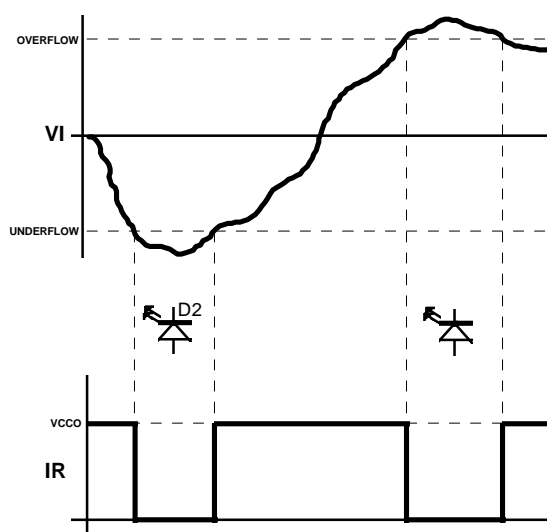
- Figure 6. IR voltage waveform -

5.4 ADC ANALOG, DIGITAL AND OUTPUT STAGES POWER SUPPLIES:

Usually, a single power supply of 5V is necessary to supply the **TDA8761AM**, but on the **Demoboard**, the ADC is evaluated with a 3.3V voltage supply of the output stages.

To ensure a good bypassing at low and high frequencies, the use of several different parallel capacitors was required and SMD bypass π type filters were implanted on the board near the ADC.

5.5 REFERENCE VOLTAGES VRB AND VRT:

The TOP Reference Voltage V_{RT} of 3.43V is obtained from a specific IC precision voltage regulator implanted on the board. The regulator output voltage is directly applied on the V_{RT} pin of the ADC, a 100nF capacitor placed close to this point constitutes an effective decoupling.

The BOTTOM Reference Voltage V_{RB} of 1.3V is obtained by the **control loop** from a specific IC low voltage operational amplifier and a transistor. The output voltage of this **control loop** is directly applied on the V_{RB} pin of ADC.

6. ENVIRONMENT CIRCUITS:

6.1 GENERAL POWER SUPPLY:

The electrical diagram is shown on **Figure 7**. Two IC voltage regulators **IC1** and **IC2** are used directly mounted on the board and they are supplied from an external DC power unit of $12V_{DC}$/220mA. Nevertheless, the external voltage can range from $10V_{DC}$ to $15V_{DC}$.
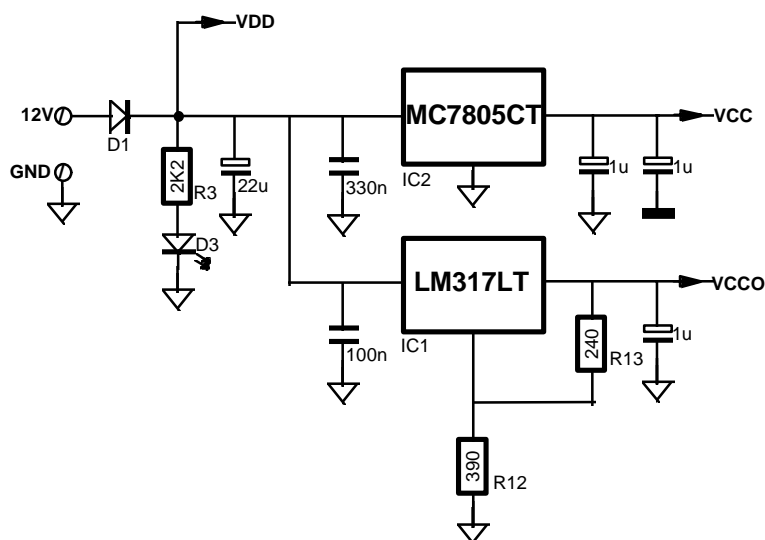
- Figure 7. Electric diagram of the power supply -

The regulation and the stabilisation of all circuitry come from the **VDD** voltage value obtained after the protection diode **D1**. Two stabilised voltages **VCC** of 5V and **VCCO** of 3.3V are available on the **Demoboard** with the distribution:

VCC used for:	VCCO used for:
Internal oscillator.	Latch interface.
ADC digital and analog supply voltages.	ADC output stages supply voltage.

The BYD17G Silicon diode **D1** ensures the protection of all the circuitry from reverse polarity, the good supply plugging is indicated by a green LED **D3**.

6.2 TOP REFERENCE VOLTAGE REGULATOR:

The precision voltage regulator **IC10 µA723CD** of PHILIPS SEMICONDUCTORS is used and mounted as a positive low-voltage regulator. The electric diagram used is shown on **Figure 8**.
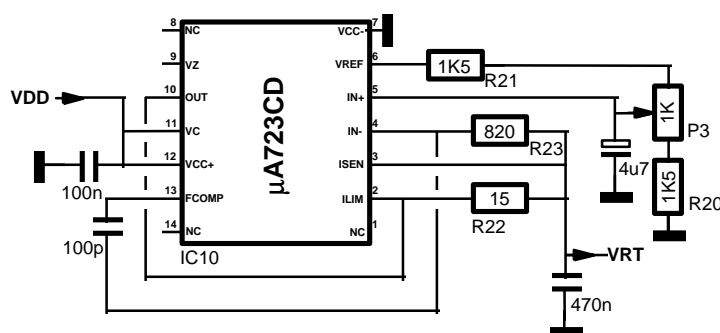
- Figure 8. Electric diagram of the TOP reference voltage -

The voltage level VDD obtained on the cathode of the protection diode **D1** is applied on the VCC+ (pin 12) of this device.

The nominal reference level of 3.43V is obtained from the voltage level supplied on the VREF (pin 6) of the **µA723CD**. A bridge resistor **R20** and **R21** with a potentiometer **P3** allows to adjust the reference level value on the no-inverting input IN+ (pin 5) of the IC.

The frequency compensation of the output current amplifier stage is done with an external capacitor of 100pF connected between FCOMP (pin 13) and IN- (pin4).

6.3 BOTTOM REFERENCE VOLTAGE:

The low voltage operational amplifier **IC7 NE5230D** associated with the transistor PNP **T1 BC859C** of PHILIPS SEMICONDUCTORS is used and mounted as a control loop stage. The electric diagram used is shown on **Figure 9**.
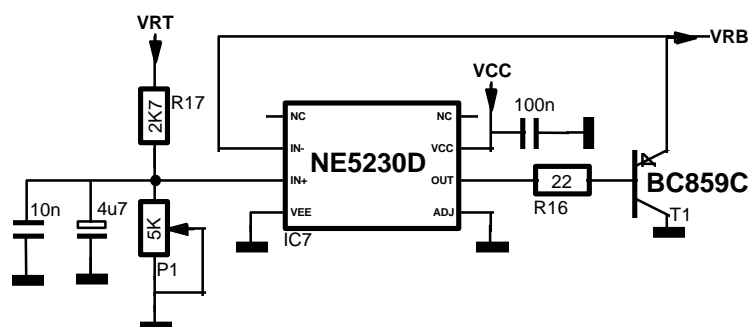
- Figure 9. Electric diagram of the BOTTOM reference voltage -

The V_{RB} voltage, controlled by the trimmer potentiometer **P1**, is connected on IN+ of **IC7** and is compared to IN- reference voltage of ADC to compensate the different thermal variations of the voltage values due to the quantization ladder.

The voltage output of the operational amplifier allows to control the conduction of the transistor **T1** which drives the current of the quantization ladder to GND. A resistor **R16** is therefore provided on the board to limit the output current in **IC7**.

6.4 CLOCK JITTER:

The jitter value of the clock signal must be low otherwise some sampling errors can appear. The jitter value can be calculated from the slope of the sinewave input signal. The sinewave input signal is given by:

$$\mathbf{v(t)} = \frac{\mathrm{v_{iFS}}}{2}.\mathbf{sin(2.\textit{p}.f_i.t)} \text{ ,}$$

where:

$\mathrm{v_{iFS}} = 2^n.q$: ADC full scale,

n   : ADC bit number,

f_i : input signal frequency.

Hence, the slope of the sinewave is:

$$\Delta\mathbf{v(t)} = \Delta\mathbf{t}.\frac{\P\mathbf{v(t)}}{\P t} = \Delta\mathbf{t}.\frac{\mathrm{v_{iFS}}}{2}.\mathbf{2.\textit{p}.f_i}.\mathbf{cos(2.\textit{p}.f_i.t)} \text{ .}$$

The slope is maximum at $t_0=0$ (middle of the input full scale):

$$\Delta\mathbf{v(t_0)} = \Delta\mathbf{t_0}\cdot\mathrm{v_{iFS}}\cdot\textit{\textbf{p}}\cdot\mathbf{f_i} \text{ ,}$$

hence:

$$\Delta t_0 = \frac{\Delta v(t_0)}{2^n.q.\textit{p}.f_i} \text{ .}$$

For a jitter below the quantum ($\Delta v(t_0) = q$), it is inferior at:

$$\Delta\mathbf{t_0} < \mathbf{62ps,}$$

with:

n = 9, f_i = 10MHz.

The variation around the frequency of the sampling clock is given by:

$$\frac{\Delta f_{clk}}{f_{clk}} = \frac{\dfrac{\Delta t_0.f_{clk}}{2}}{1-\left(\dfrac{\Delta t_0.f_{clk}}{2}\right)^2} \text{ ,}$$

hence:

$$\frac{\mathbf{\Delta f_{clk}}}{\mathbf{f_{clk}}} \langle \pm\mathbf{1240ppm} \text{ ,}$$

where:

f_{clk} = 40MHz.

6.5 CLOCK OSCILLATOR:

On the **Demoboard,** a specific circuit is designed to produce the clock signal addressed to the ADC and to the latch interface circuit with the Motorola IC "ECL in PS" family. This is used to design a PECL mounting crystal oscillator. The electric diagram is shown on **Figure 10**.
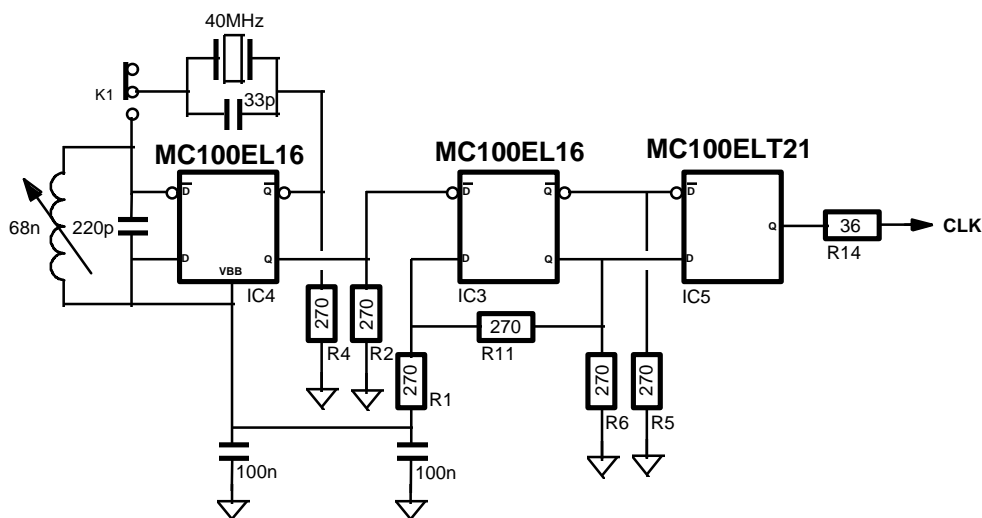
- Figure 10. Electric diagram of the clock oscillator -

Two differential receivers **MC100EL16** are used to make the function of oscillating and shaping. The first differential receiver is associated in positive feedback with the quartz of 40MHz ±100ppm. The antiresonance harmonic frequency is selected from the tuned inductance of 68nH of the tank circuit 68nH-220pF.

The first differential receiver output drives the input of the Schmitt trigger circuit constituted by the second differential receiver **IC3** and by the associated resistors **R1** and **R11**. The second differential receiver output drives the **IC5** differential PECL to the TTL translator **MC100ELT21**.

The **R14**=36Ω resistors is used to improve the clock signal.

Advice:

Usually, in some applications where the clock signal is not adapted, it is necessary to put a resistor, far of the ADC clock input, on the clock signal line. This resistor allows to eliminate principaly the undershoot which device does not like, and to improve the clock signal.

The waveforms, with and without **R14**, of the clock oscillator signal obtained at 40Msps are shown on **Figure 11**.
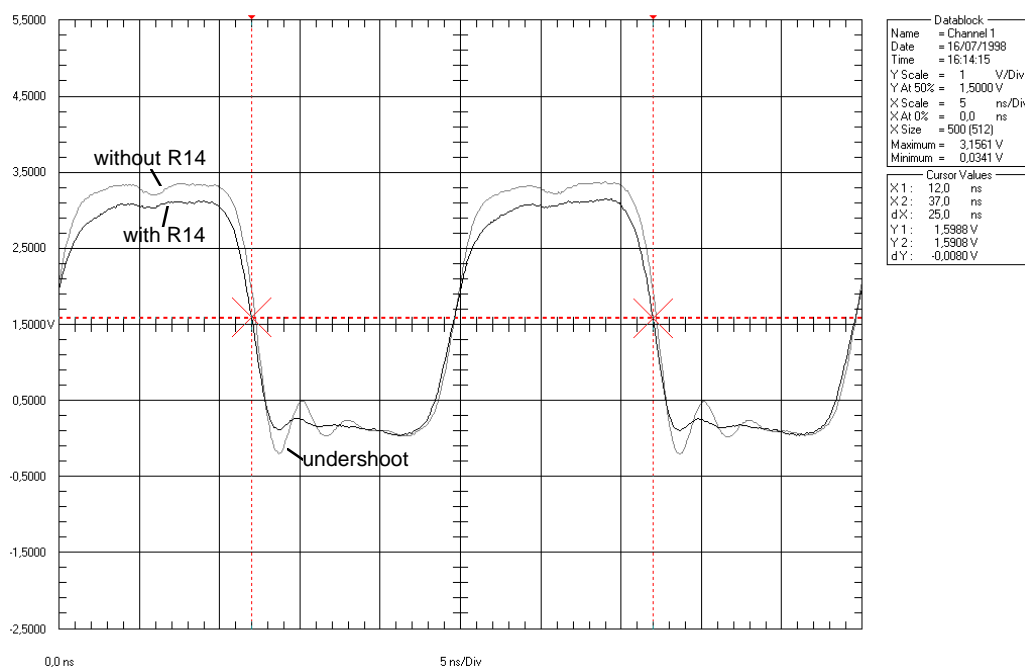
- FIGURE 11. Clock oscillator waveforms -

6.6 CLOCK SELECTOR CIRCUIT:

The position of the **K1** and **K3** switches 1C/2P on the **Demoboard** must be set on respectively **ON** and **INT** to use the internal clock oscillator, and on **OFF** and **EXT** to use the external generator which is connected to **J2** SMA connector.

To avoid the crosstalk when the external CLK is used, do not forget to switch off K1.

6.7 LATCH INTERFACE:

The electric diagram of the latch interface is shown on **Figure 12**. It allows to recover the ADC data output synchronized on the clock sampling.
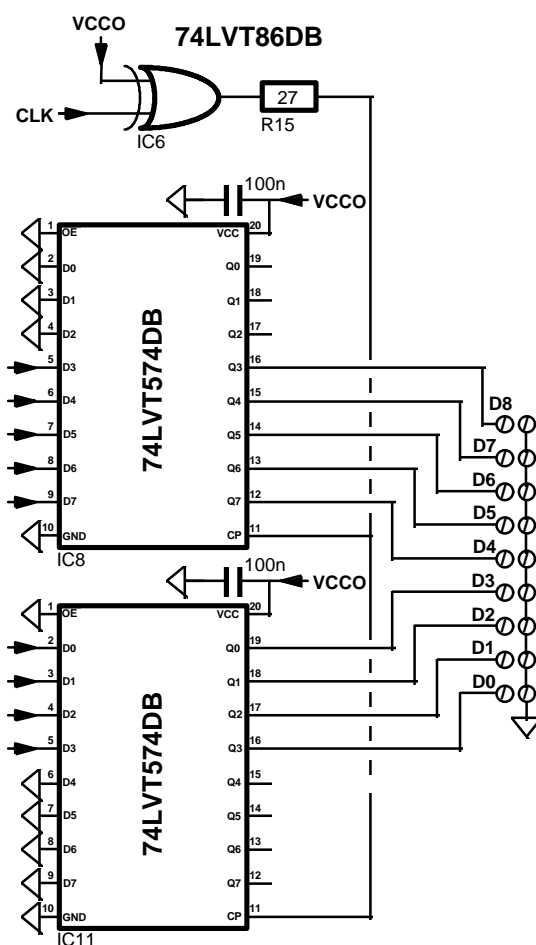
- Figure 12. Electric diagram of the latch interface -

The interface circuit uses two SMD ICs D-type flip-flop **74LVT574DB** from the Low Voltage Technology logic family.

The **R15**=27Ω resistors is used to improve the clock signal.

7. OPERATING MODE:

An external power unit of 12V/220mA is required to supply the **Demoboard**. However, the board is able to work between 10 V and 15 V.

All DC voltage adjustments of **P3** (V_{RT}), **P1** (V_{RB}) and **P2** (V_{OFS}) are locked in the laboratory before delivery to be true to the provided product specifications.

So:

$$V_{RT} \ = \ 3.43V,$$

$$V_{RB} \ = \ 1.30V,$$

$$V_{OFS} = \ 2.365V.$$

But the V_{OFS} value may be modified by the user to obtain the best full scale of the input analog signal. To do this, it is better to use the IR viewer to check if the analog input signal is out of range. In this case, the LED **D2** lightes on.

Before putting the board on, please check that **K1** is **OFF**, **K2** and **K4** are **ON**, and **K3** is **INT** (referring to the implantation diagram given on **Figure 3**).

7.1 INTERNAL CLOCK OPERATION:

In this mode, the different positions of the switches are given on **Figure 13**. To switch **ON** the internal clock oscillator, use switch **K1** once the board is powered on.
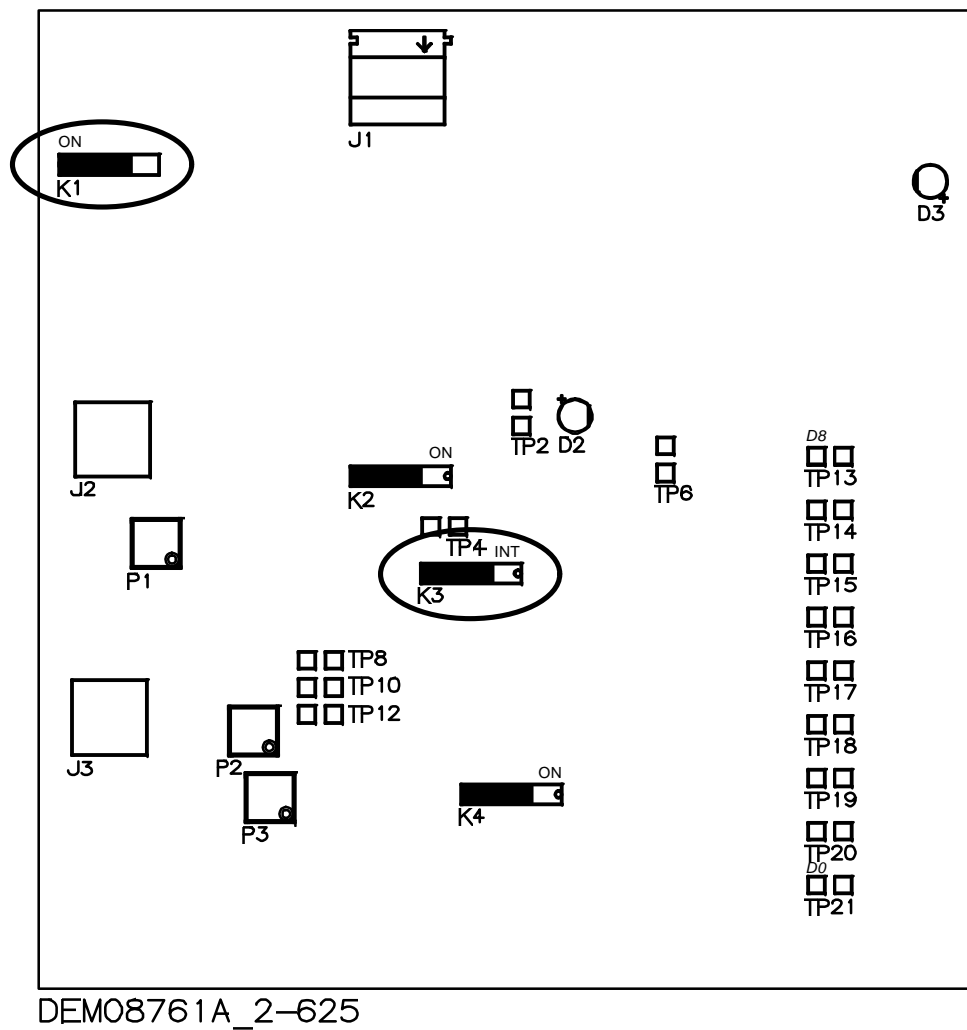
- Figure 13. Board configuration using the clock oscillator -

7.2 EXTERNAL SINGLE CLOCK OPERATION:

In this mode, the position of the different switches and the location of the connector are given on **Figure 14**.

- The internal clock oscillator command is set on **OFF** with the switch **K1** to avoid crosstalk.
- The external clock oscillator is set on **EXT** with the switch **K3**.
- The 50Ω SMA connector **J2** is used to connect the external 50Ω square clock generator.

DEM08761A_2-625
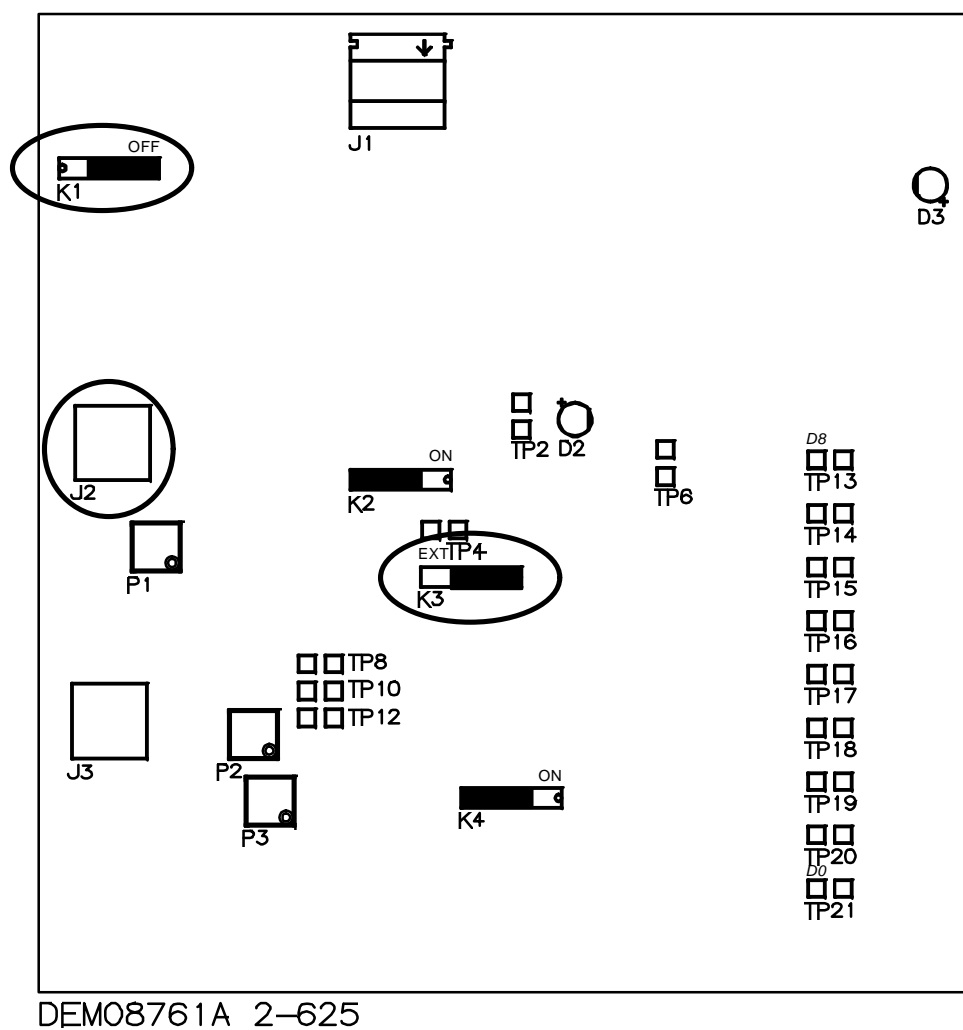
- Figure 14. Board configuration using an external clock -

The required clock levels are:

$$V_{CLKH} \, min = 2.0V,$$

$$V_{CLKL} \, max = 0.8V.$$

7.3 QUICKVIEW OF THE DEMOBOARD:

A quick view of the **TDA8761AM Demoboard** with main information is given on **Figure 15**.

DEMO8761A_2−625
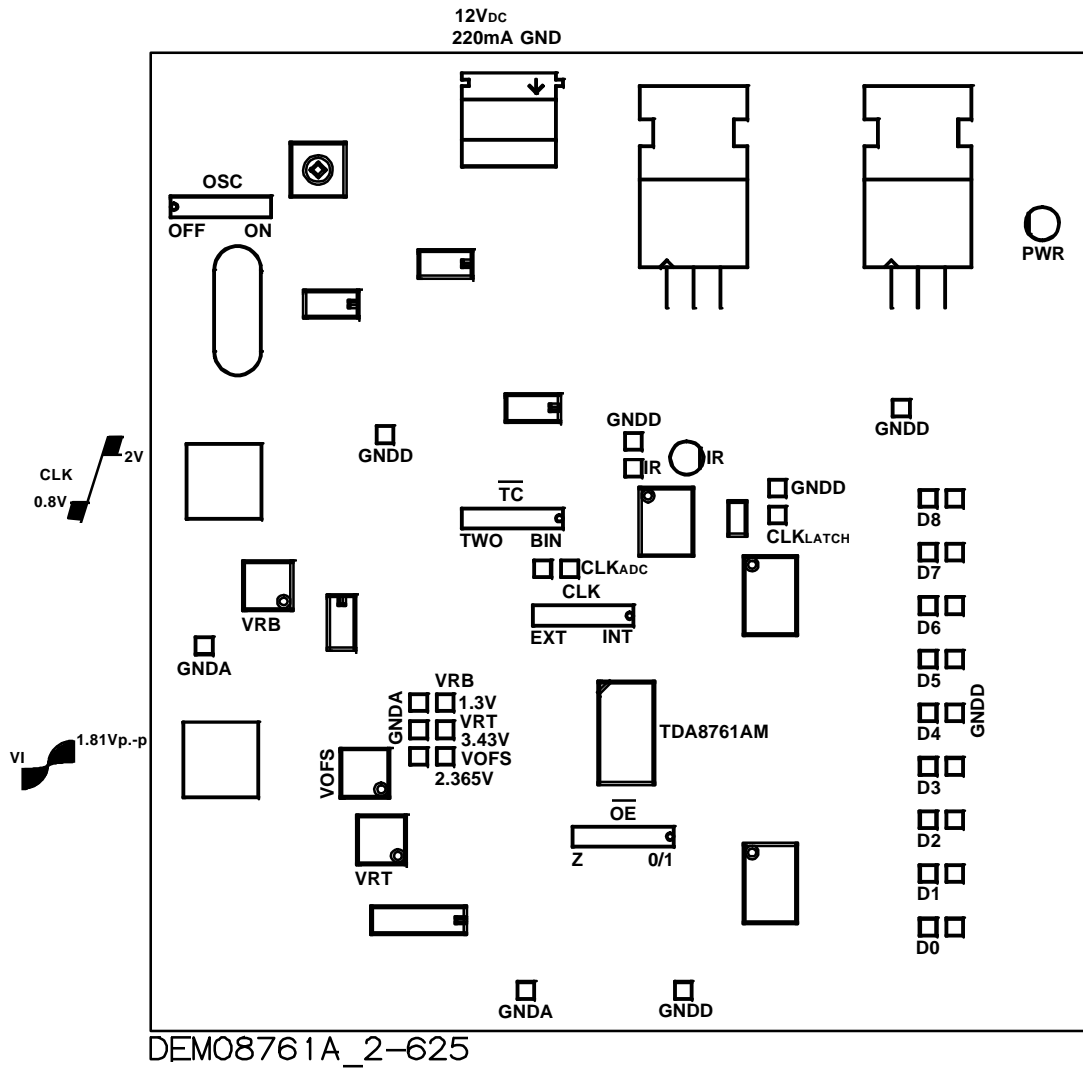
- *Figure 15. Quickview of the TDA8761AM Demoboard version with main information -*

8. PERFORMANCES:

An evaluation of the **TDA8761AM** ADC performances were made with the **Demoboard** environment on CAEN's dynamic bench.

8.1 DEFINITION OF THE MEASURING PARAMETERS:

To evaluate the ADC performances on the Demoboard, the CAEN dynamic bench uses the **F**ast **F**ourier **T**ransform for dynamic parameters and the **Histogram** for *static* parameters from the sample signal.
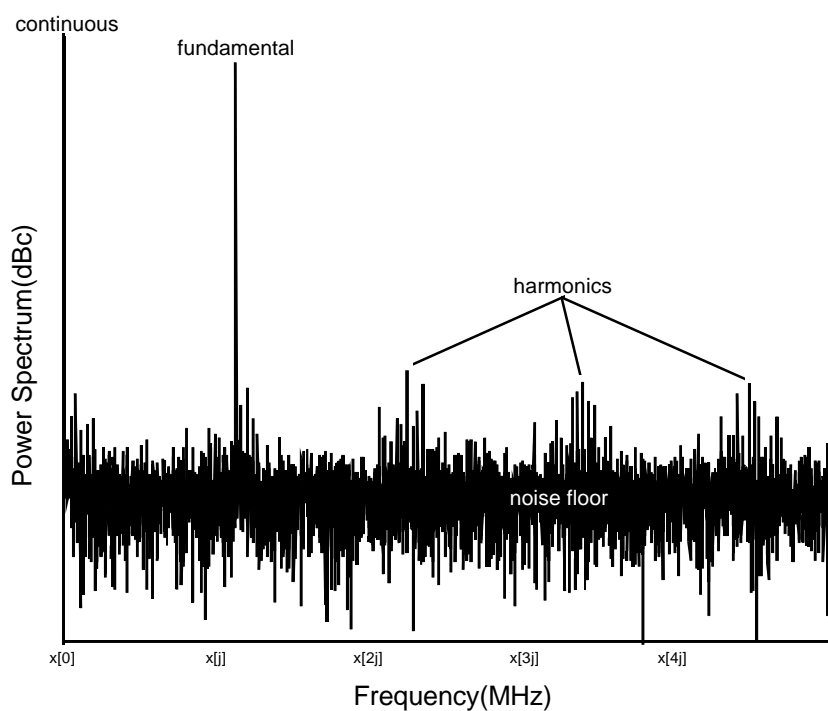
- Figure 16. FFT -

According to the FFT shown on **Figure 16**, the main dynamic parameters are:

- The **T**otal **H**armonic **D**istortion is the ratio between the RMS signal amplitude and the RMS sum of the first five harmonics. From the power spectrum of FFT, the **THD** is calculated from the relation:

$$\text{THD}_{\text{dBc}} = 20 \times \log_{10} \frac{\text{x}[\text{j}]}{\sqrt{\sum_{\text{i}=2}^{6} \text{x}^2[\text{i} \times \text{j}]}} \, .$$

Where:

   x[j] : fundamental component corresponding with the j spectrum component,

   x[i × j] : component of harmonic i.

- The **S**purious **F**ree **D**ynamic **R**ange is the ratio between the RMS signal amplitude and the RMS value of the highest spectrum component (harmonic or noise). From the FFT, the **SFDR** is calculated from the relation:

$$\text{SFDR}_{\text{dB}} = 20 \times \log_{10} \frac{\text{x}[\text{j}]}{\text{MAX}(\text{x}[\text{i}])} \, .$$

Where:

   x[i] : spectrum component i with $\text{i} \in [2{:}\dfrac{\text{N}}{2}]$ (N: number of samples) and $\text{i} \neq \text{x}[\text{j}]$.

- The **SI**gnal to **N**oise **A**nd **D**istortion ratio is the ratio between the RMS signal amplitude and the RMS sum of all the other spectral components. From the FFT, the **SINAD** is calculated from the relation:

$$\text{SINAD}_{\text{dB}} = 20 \times \log_{10} \frac{\text{x}[\text{j}]}{\sqrt{\sum_{\text{i}=2, \text{i} \neq \text{j}}^{\frac{\text{N}}{2}} \text{x}[\text{i}]}} \, .$$

- The **S**ignal to **N**oise **R**atio is the ratio between the RMS signal amplitude and the RMS sum of all the other spectral components without harmonic used in the **THD** relation. From the FFT, the **SNR** is calculated from the relation:

$$SNR_{dB} = 20 \times \log_{10} \frac{x[j]}{\sqrt{\sum\limits_{i=2, i \neq j \times [1:6]}^{\frac{N}{2}} x[i]}} \ .$$

- The **E**ffective number of bit is calculated by the relation (valid to NYQUIST condition):

$$E_{BIT} = \frac{SINAD - 10 \times \log_{10} \frac{3}{2}}{20 \times \log 2} \ .$$

The main *static* parameters are:

- The **D**ifferential **N**on**L**inearity is the difference between the measured width and the ideal width that is 1 LSB of a code i. Only the maximum and the minimum values are given.

- The **I**ntegral **N**on**L**inearity is the difference between the measure of the transition and of the ideal transition size of two consecutive codes. Only the maximum and the minimum values are given. The INL is calculed from the DNL following the relation:

$$INL[i] = \sum_{j=0}^{i} DNL[j],$$

where:

$i \in [0 : 2^N - 1]$ (N: number of bit).

8.2 MEASUREMENT AT 30MSPS:

The **Demoboard** is evaluated with the following measurement conditions:

Input frequency:	9.96MHz.
Waveform:	Sinewave.
Magnitude:	Full Scale (FFT), Full Scale +5% (DNL/INL).
Antialiasing Filter:	Yes
Clock frequency:	30Msps.
Operating mode:	External clock.

The typical results and the corresponding diagrams obtained under these conditions are given on **Figures 17 and 18**.

FFT: Size: 4096samples/f_{clk}: 30MSPS/f_i: 9.968261719MHz

1f_i: 9.97MHz: 0dBc   THD: 59.98dBc
2f_i: 10.1MHz: -68.28dBc   SFDR: -63.13dBc
3f_i: 0.09MHz: -68.13dBc   SINAD: 52.72dB
4f_i: 9.87MHz: -67.46dBc   SNR: 53.63dB
5f_i: 10.2MHz: -63.13dBc   E: 8.46bit
6f_i: 0.19MHz: -74.56dBc
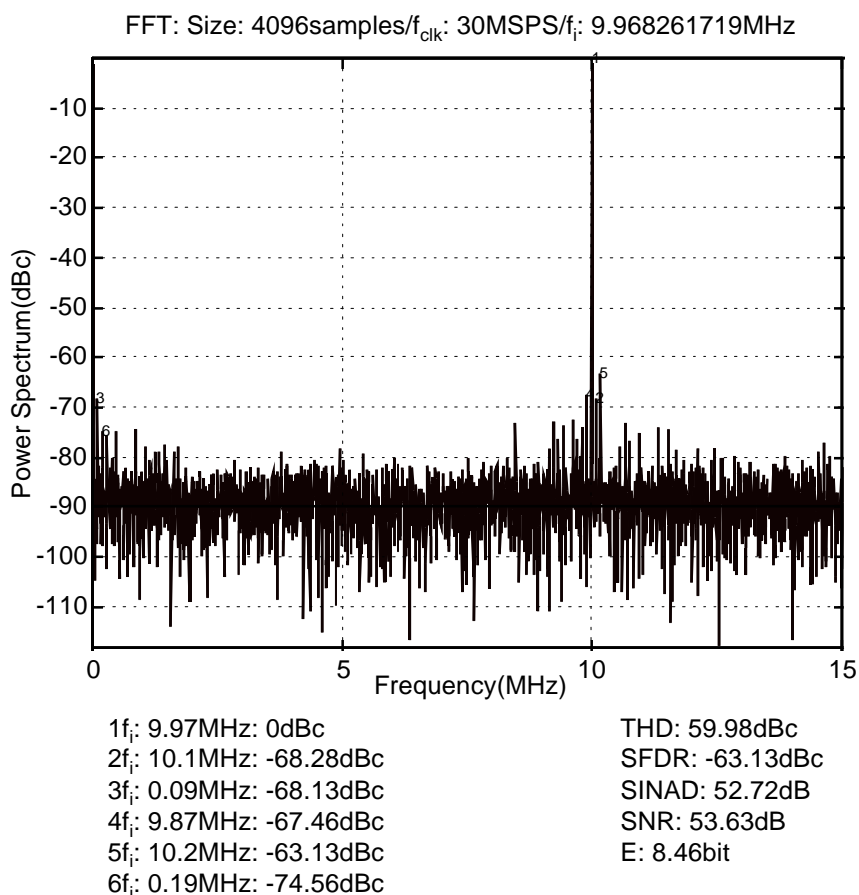
- Figure 17. FFT results of the 30Msps -

Differential NonLinearity: f_{clk}: 30MSPS/f_i: 9.987487793MHz

Integral NonLinearity: f_{clk}: 30MSPS/f_i: 9.987487793MHz
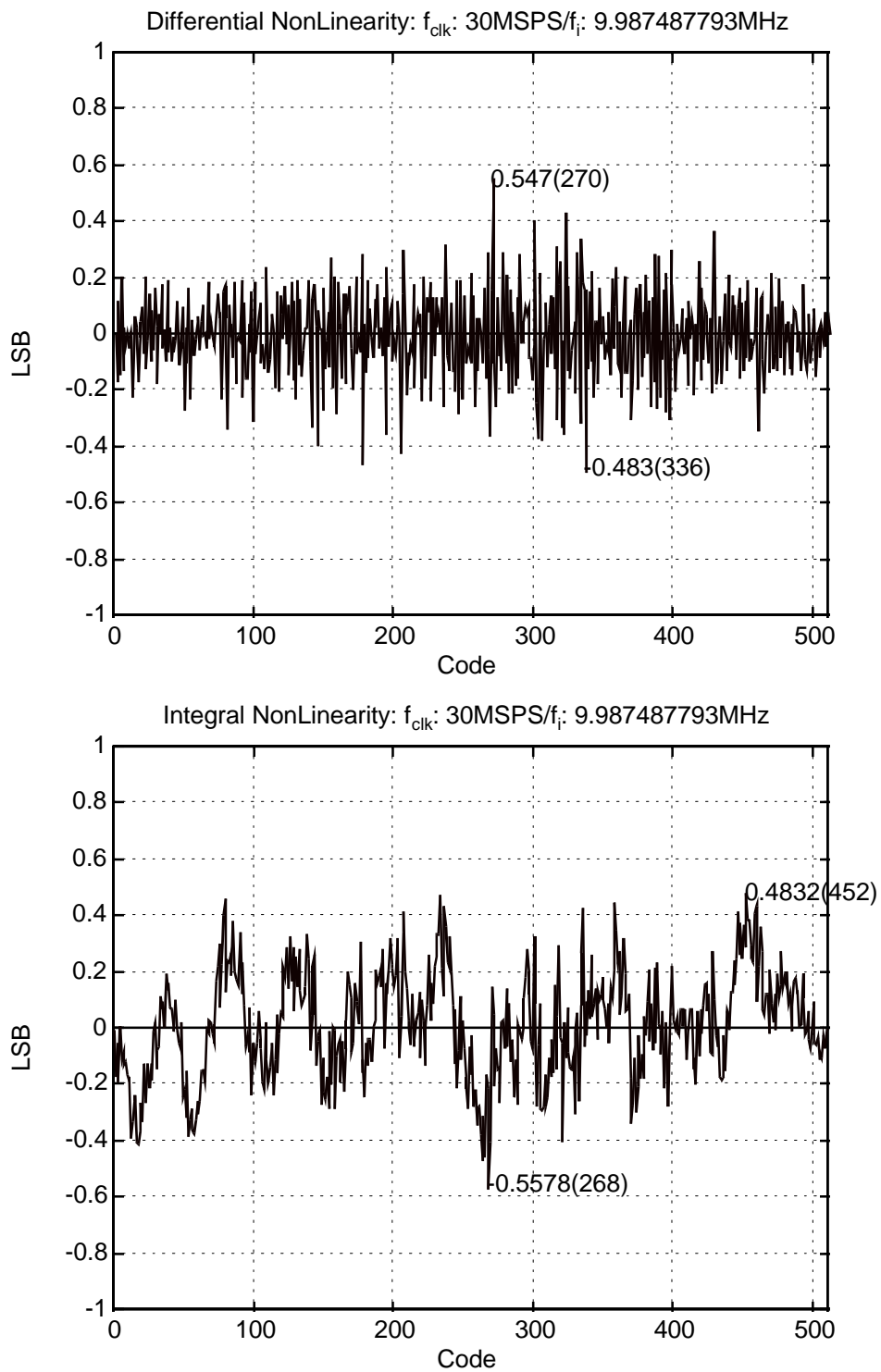
- Figure 18. DNL and INL results of the 30Msps -

8.3 MEASUREMENT AT 40MSPS:

This version of the **Demoboard** is evaluated with the following measurement conditions:

Input frequency:	9.97MHz.
Waveform:	Sinewave.
Magnitude:	Full Scale.
Antialiasing Filter:	Yes
Clock frequency:	39.99Msps.
Operating mode:	Internal clock.

The typical results and the corresponding diagrams obtained under these conditions are given on **Figure 19**.

FFT: Size: 4096samples/f_{clk}: 39.997085MSPS/f_i: 9.96997651MHz

1f_i: 9.97MHz: 0dBc   THD: 57.46dBc
2f_i: 19.9MHz: -59.88dBc   SFDR: -59.88dBc
3f_i: 10.1MHz: -64.6dBc   SINAD: 51.49dB
4f_i: 0.12MHz: -74.37dBc   SNR: 52.76dB
5f_i: 9.85MHz: -64.42dBc   E: 8.26bit
6f_i: 19.8MHz: -76.95dBc
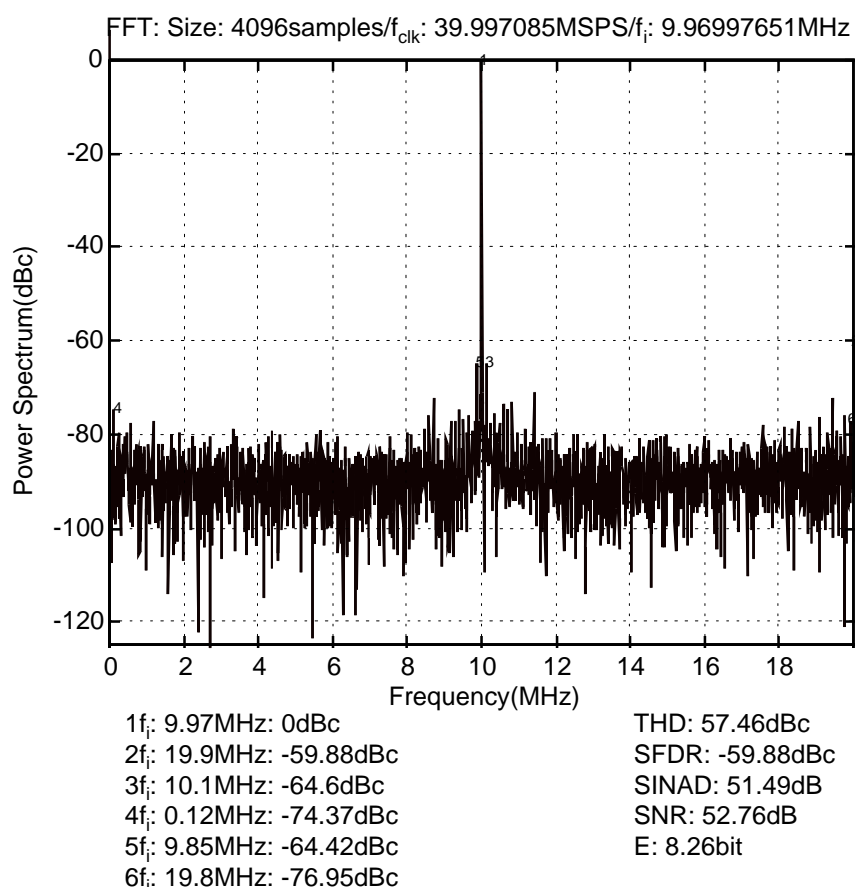
- Figure 19. FFT results of the 40Msps with clock oscillator of Demoboard -

9. DEMOBOARD FILES:

All documents needed for the realization of this **Demoboard** are given on **Figures 20 to 27**.

- Electrical diagram.
- Topside component implantation.
- Underside component implantation.
- Topside component layout 1.
- Internal layout ground layout 2.
- Internal layout supply layout 3.
- Internal layout ground layout 4.
- Underside component layout 5

The components list with their values and references is given on **Table 1 to 4**.
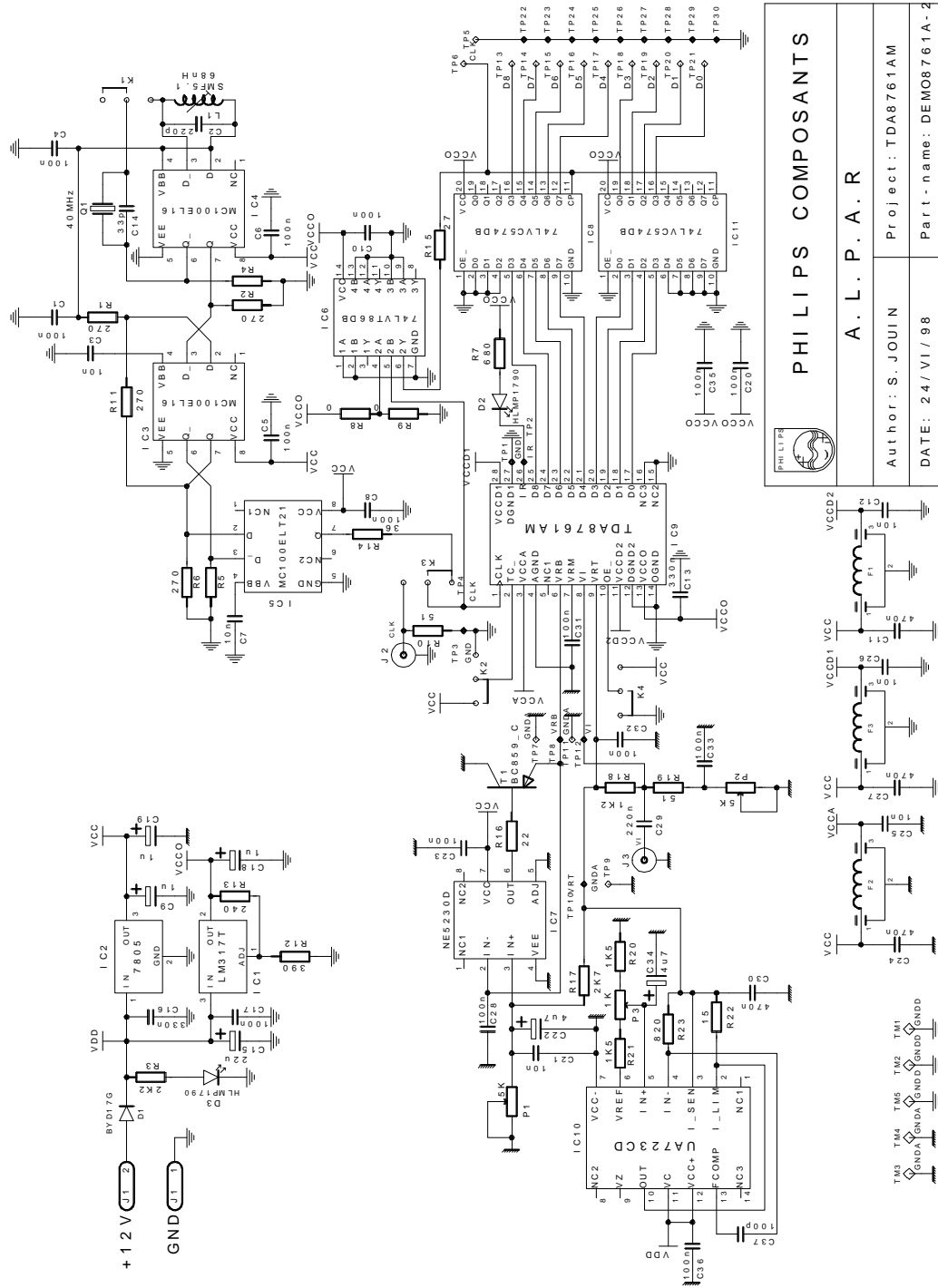
- Figure 20. Demoboard electrical diagram -
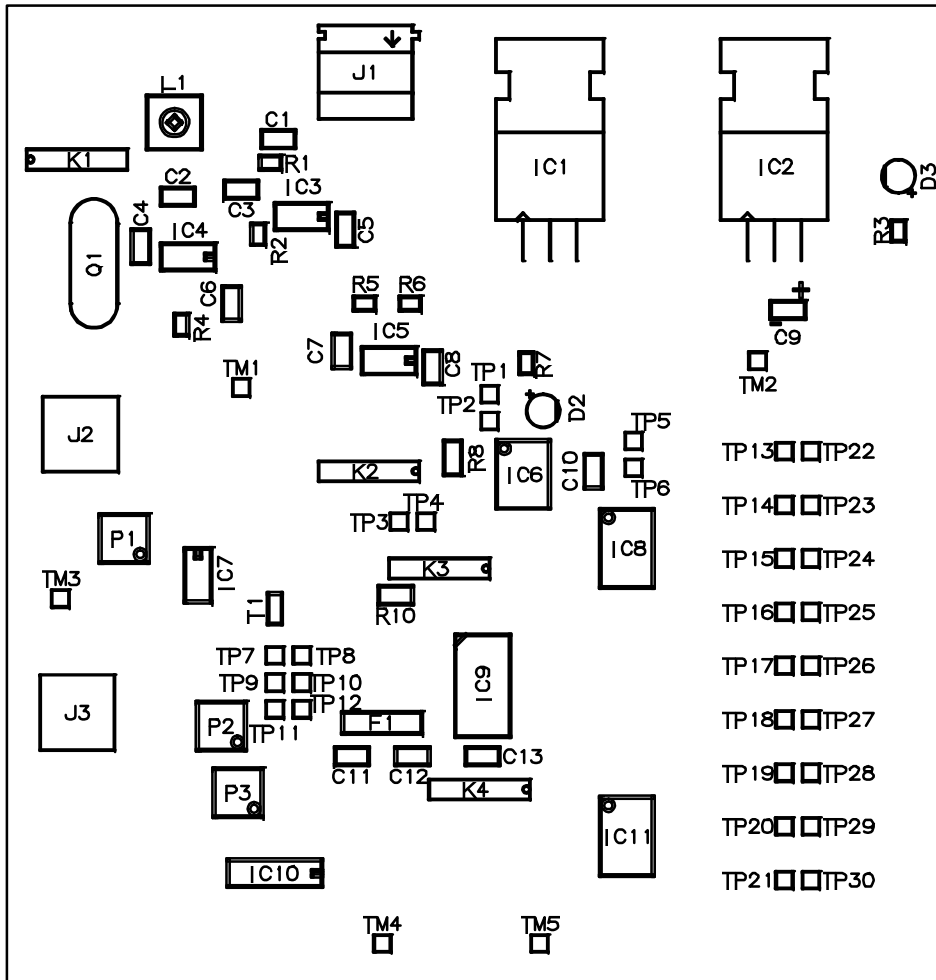
- Figure 21. Topside component implantation -
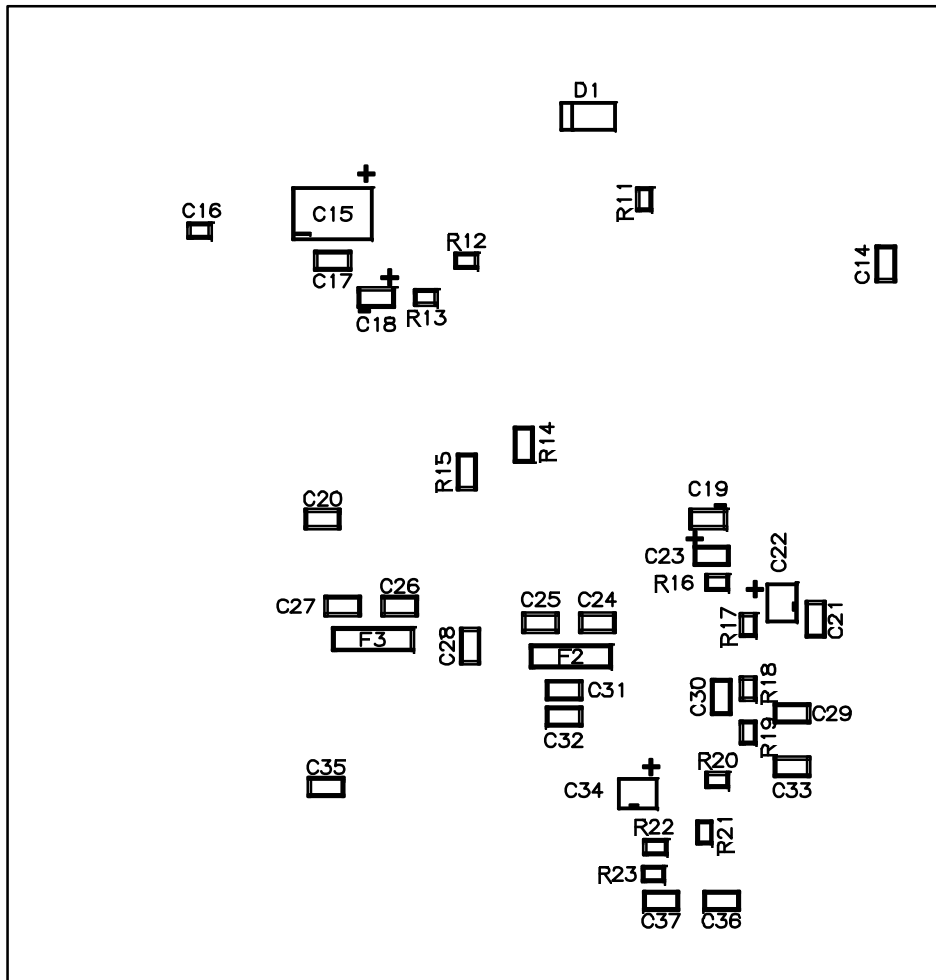
- Figure 22. Underside component implantation -
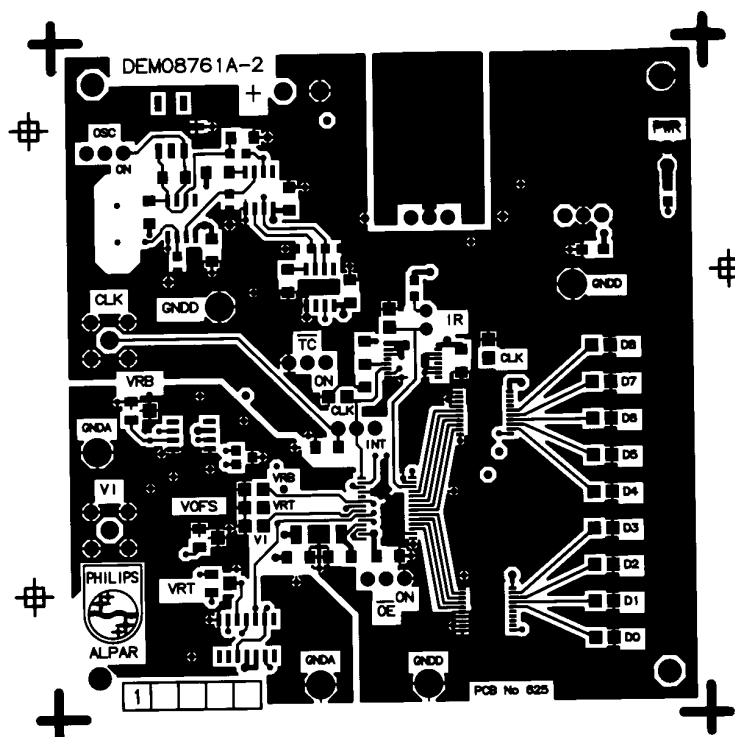
- Figure 23. Topside component layout (signal layer 1) -

- Figure 24. Internal plane layout (ground layer 2) -

- Figure 25. Internal layout (supply layer 3) -
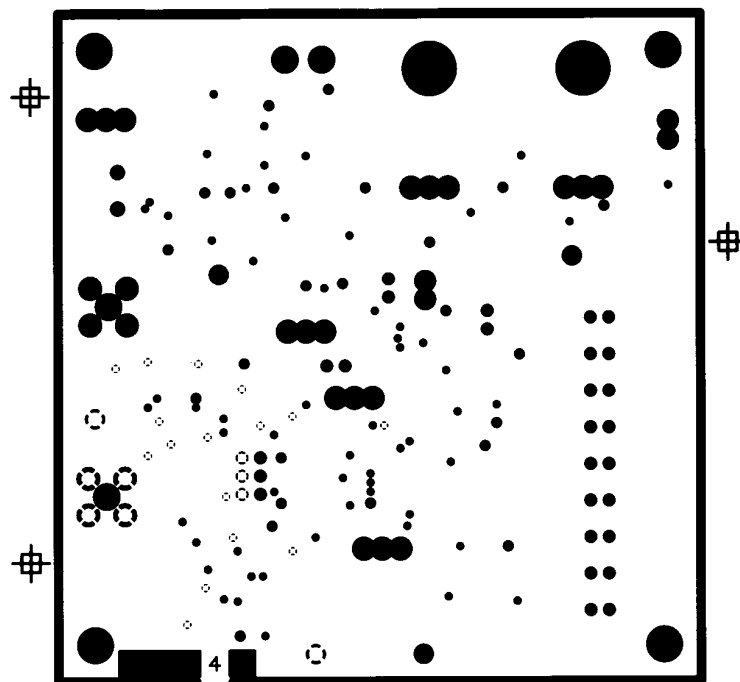
- Figure 26. Internal plane layout (ground layer 4) -
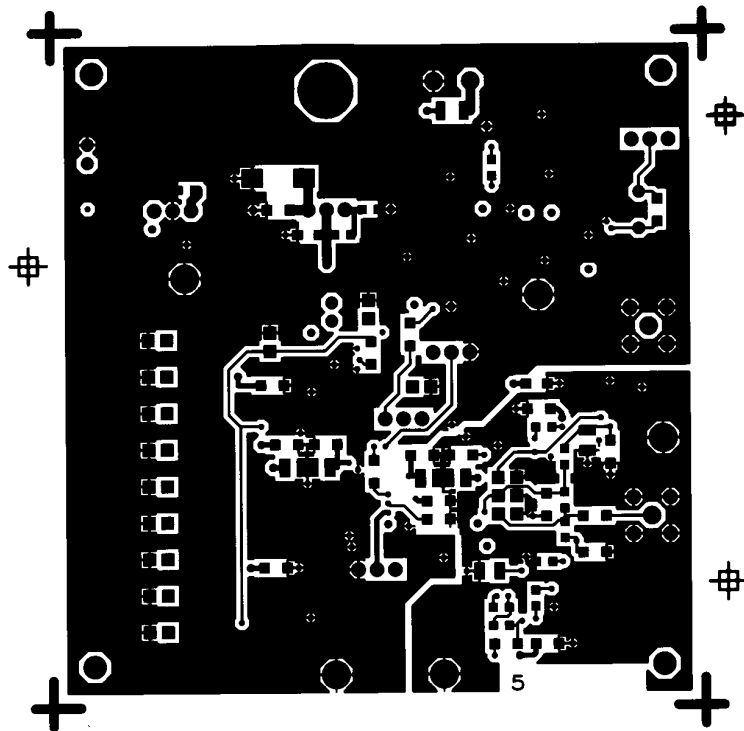
- Figure 27. Underside component layout (signal layer 5) -

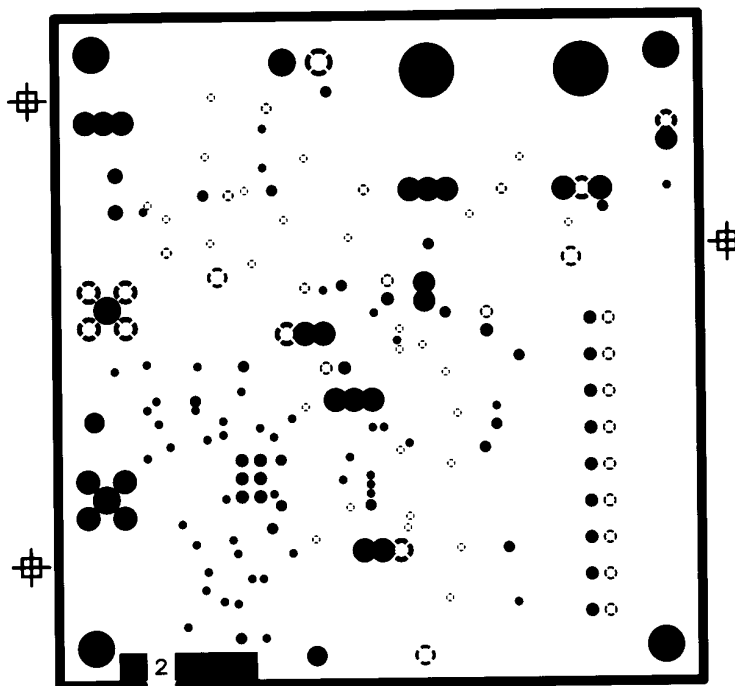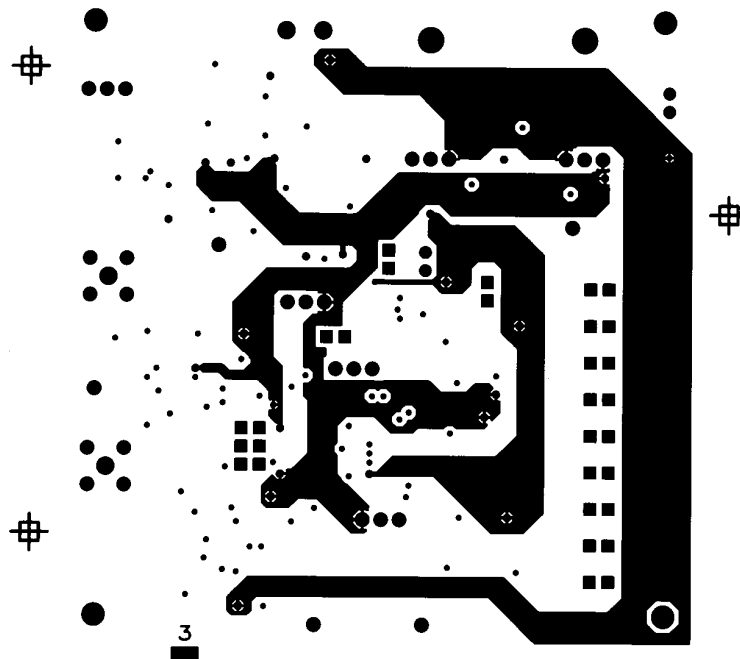| REF	VALUE	COMPONENT	TYPE	MANUFACTURER
C1	100nF	CAPACITOR	C1206	PHILIPS
C2	220pF	'	'	'
C3	10nF	'	'	'
C4	100nF	'	'	'
C5	100nF	'	'	'
C7	10nF	'	'	'
C8	100nF	'	'	'
C9	1µF/16V	'	293D/A	SPRAGUE
C10	100nF	'	C1206	PHILIPS
C11	470nF	'	'	'
C12	10nF	'	'	'
C13	330nF	'	'	'
C14	33pF	'	'	'
C15	22µF/16V	'	293D/D	SPRAGUE
C16	330nF	'	C0805	PHILIPS
C17	100nF	'	C1206	'
C18	1µF/16V	'	293D/A	SPRAGUE
C19	1µF/16V	'	'	'
C20	100nF	'	C1206	PHILIPS
C21	10nF	'	'	'
C22	4.7µF/16V	'	293D/B	SPRAGUE
C23	100nF	'	C1206	PHILIPS
C24	470nF	'	'	'
C25	10nF	'	'	'
C26	10nF	'	'	'
C27	470nF	'	'	'
C28	100nF	'	'	'
C29	220nF	'	'	'
C30	470nF	'	'	'
C31	100nF	'	'	'
C32	100nF	'	'	'
C33	100nF	'	'	'
C34	4.7µF/16V	'	293D/B	SPRAGUE
C35	100nF	'	C1206	PHILIPS
C36	100nF	'	'	'
C37	100pF	'	'	'
D1		DIODE	BYD17G	PHILIPS
D2		RED LED	HLMP1790	HEWLETT PACKARD
D3		GREEN LED	'	'

- Table 1. List of components -

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
F1	2nF	Π FILTER	4700-003-S	TUSONIX
F2	2nF	'	'	'
F3	2nF	'	'	'
IC1		ADJUSTABLE REGULATOR	LM317T	TEXAS INSTRUMENTS
IC2		VOLTAGE REGULATOR	T7805CT	MOTOROLA
IC3		LINE RECEIVER	MC100EL16	'
IC4		'	'	'
IC5		PECL TO ECL TRANSLATOR	MC100ELT21	'
IC6		EXCLUSIVE-OR	74LVT86DB	PHILIPS
IC7		LOW VOLTAGE OP. AMPLI.	NE5230D	'
IC8		D TYPE FLIP FLOP	74LVT574DB	'
IC9		ADC	TDA8761AM	'
IC10		PRECISION VOLTAGE REG.	UA723CD	'
IC11		D TYPE FLIP FLOP	74LVT574DB	'
J1		CONNECTOR	MKSD	PHOENIX
J2	50Ω	'	SMA	RADIALL
J3	50Ω	'	'	'
K1		SWITCH	1C2P	SECME
K2		'	'	'
K3		'	'	'
K4		'	'	'
L1	68nH	SELF	SMF5.1	NEOSID
P1	5KΩ	POTENTIOMETER	3224W	BOURNS
P2	5KΩ	'	'	'
P3	1KΩ	'	'	'
Q1	40MHz	QUARTZ	HC49U	KONY
R1	270Ω	RESISTOR	0805	PHILIPS
R2	270Ω	'	'	'
R3	2.2kΩ	'	'	'
R4	270Ω	'	'	'
R5	270Ω	'	'	'
R6	270Ω	'	'	'
R7	680Ω	'	'	'

- Table 2. List of components -

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
R8	0Ω	RESISTOR	1206	PHILIPS
R9	**Do not solder**	'	'	'
R10	51Ω	'	1206	'
R11	270Ω	'	0805	'
R12	390Ω	'	'	'
R13	240Ω	'	'	'
R14	36Ω	'	1206	'
R15	27Ω	'	'	'
R16	22Ω	'	0805	'
R17	2.7kΩ	'	'	'
R18	1.2kΩ	'	'	'
R19	51Ω	'	'	'
R20	1.2kΩ	'	'	'
R21	1.5kΩ	'	'	'
R22	15Ω	'	'	'
R23	820Ω	'	'	'
TM1		MEASUREMENT POINT		COMATEL
TM2		'		'
TM3		'		'
TM4		'		'
TM5		'		'
TP1		TEST POINT		COMATEL
TP2		'		'
TP3		'		'
TP4		'		'
TP5		'		'
TP6		'		'
TP7		'		'
TP8		'		'
TP9		'		'
TP10		'		'
TP11		'		'
TP12		'		'
TP13		'		'
TP14		'		'
TP15		'		'
TP16		'		'
TP17		'		'

- Table 3. List of components -

- TDA8761AM -

DEMONSTRATION BOARD

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
TP18		TEST POINT		COMATEL
TP19		'		'
TP20		'		'
TP21		'		'
TP22		'		'
TP23		'		'
TP24		'		'
TP25		'		'
TP26		'		'
TP27		'		'
TP28		'		'
TP29		'		'
TP30		'		'

- Table 4. List of components -